

bc330SBX
Time Code Translator
8500-0004

User's Guide

Rev B
(June 30, 2000)

**bc330SBX
TIME CODE TRANSLATOR**

TABLE OF CONTENTS

SECTION	PAGE
----------------	-------------

**ADDENDUM A
OUTPUTS**

A.0 J2 Serial RS-422 Differential Output.....	A-1
A.1 bc330SBX RS-422 Serial Output Messages	A-1

**CHAPTER ONE
INTRODUCTION**

1.0 Scope.....	1-1
1.1 Functional Description.....	1-1
1.2 Electrical Description.....	1-2
1.3 Mechanical Description.....	1-4
1.4 Level of Compliance	1-4

**CHAPTER TWO
ADDRESS SPACE**

2.0 Control Address Space.....	2-1
2.1 Data Transfer Address Space.....	2-2
2.2 Latency.....	2-4

**CHAPTER THREE
DATA AND CONNECTOR ASSIGNMENTS**

3.0 Using Timecode Period Data.....	3-1
3.1 Serial Port Data	3-2
3.2 SBX Connector Assignments (P2).....	3-2

TABLE OF CONTENTS

**CHAPTER FOUR
ADJUSTMENT**

4.0 Adjustment 4-1

**CHAPTER FIVE
DRAWINGS**

5.0 Drawings 5-1

**CHAPTER SIX
PARTS LIST**

6.0 Parts List..... 6-2

ADDENDUM A

OUTPUTS

A.0 J2 SERIAL RS-422 DIFFERENTIAL OUTPUT

A serial RS-422 differential output is available on the edge connector labeled “P1” pin 22 and pin 24. A twisted pair wires can be used with P1-22 and P1-24. This output port can be used for diagnostic purposes. The bc330sbx broadcasts time, measured code period, code detection status, code search status, software version and date code, AGC slice level, and control byte information. Data is sent at 9600 baud, eight data bits, one stop bit, no parity. Each line is terminated by a carriage return (ODH) and a line feed (OAH).

The Tx(-) signal will drive most RS-232 interfaces such as a serial port to a PC. The data pacing signals RTS, CTS, DSR and DTR may need to be jumpered depending on the specific terminal emulation software in use.

A.1 BC330SBX RS-422 SERIAL OUTPUT MESSAGES

When a valid time code signal is being decoded, a packet of data is sent every second, about ½ second after the 1pps signal occurs. The following are examples of message data when decoding the respective time code signals, real time clock and other time sources:

Initialization Message

```
SLAMR bc330sbx x.x dd/mm/yr
initialization complete
control bytes 0/1/2 = XX/XX
hb period remainder = XXXX XXXX
```

Decoding Modulated Time Code

```
(Time code type)          { irigb, 2137}
lev = XX                   {X represents a hexadecimal digit}
dif = XXXX
buf2 ddd hh:mm:ss
etim ddd hh:mm:ss :: :: ::
```

Searching For Time Code With Time Code Select Register Set For Autodetect

```
checking (time code type)  {Modulated time code: irigb, 2137}
lev = cannot find (time code type)
```

Time Code Error Message

```
decode error !!
```

Flywheeling Message

```
flywheeling !!  
buf2 ddd hh:mm:ss  
etim ddd hh:mm:ss :: :: ::
```

Notes

- “lev” is a hex representation of the “slice” level of a modulated time code. It is used to determine whether a cycle is a high or low cycle.
- “dif” is hexadecimal representation of the time code period measurement. It is used to scale the internal time. The “dif” value reflects the difference between the internal crystal and the external time signal.
- No control codes or commands are accepted by the user through the RS-422 port.
- The RS-422 messages were provided primarily for diagnostic purposes. The user, however, may use the data to obtain time externally from the board. Once a valid time code is being decoded, time/message data is broadcast once each second about 1/2 second after the 1pps signal. The time being broadcast, following the “buf2” label, is valid at the rising edge of the preceding 1pps pulse.

CHAPTER ONE

INTRODUCTION

1.0 SCOPE

This manual provides the information necessary to interface the bc330SBX Time Code Translator to a host environment which conforms to the SBX mechanical and electrical specifications defined in document ANSI/IEEE Standard 959-1988.

1.1 FUNCTIONAL DESCRIPTION

The bc330SBX Time Code Translator has been designed to decode the following time codes:

IRIG B - 0S 1.0
2137 - 0S 1.0

The bc330SBX has been designed to translate time codes at near real time rates, and to accept a wide range of input amplitudes and signal to noise ratios. A sophisticated 'flywheel' algorithm makes input code loss transparent to the user.

The bc330SBX module can be directed to automatically identify and translate an input code or to search only for a specified code.

The bc330SBX measures the period of the source time code to determine the rate offset of the module oscillator. This measurement is performed at a resolution of 0.5 microseconds. If the source time code is lost, the bc330SBX will continue to maintain time to the accuracy of 0.5 microseconds per second or approximately ± 5 parts in 10^7 . Temperature changes or other factors, which would cause the bc330SBX crystal to drift, will degrade this accuracy. Experience in typical laboratory environments shows that drift rates of less than a part in 10^6 are consistently achieved during periods of code loss.

The bc330SBX always assumes that the input code is accurate with respect to code rate, and 'locks' the flywheel algorithm to the measured code period.

The bc330SBX provides a hardware event strobe input which will 'log' the time of an external event to 0.5 microsecond accuracy. The CMOS logic input may be configured under software control as either positive or negative edge triggered. The occurrence of an event may be determined by polling, or the event may be programmed to generate an interrupt. Bus time requests (requests for current time) are also processed to an accuracy of 0.5 microseconds. The time is referenced to the time at which a specific bus address location is written. Both the current time and the event time output are in a packed BCD format.

CHAPTER ONE

In addition to BCD time of day, the bc330SBX outputs a one pulse per second (PPS) CMOS strobe, and a programmable CMOS pulse rate. The one PPS strobe may be advanced or retarded by up to ± 1 millisecond in steps of 0.5 microseconds to compensate for propagation delay effects.

1.2 ELECTRICAL DESCRIPTION

The bc330SBX conforms to the specifications of ANSI/IEEE Standard 959-1988, Section Three. The logic family used in the bc330SBX is CMOS, and the specific requirements for the signals in Table Six of the ANSI document are met.

Table 1-1 provides the actual electrical characteristics of the bc330SBX by signal type for the SBX bus connector (P2).

Table 1-2 provides similar data for the card edge connector signals (P1).

Table 1-3 defines the signals on the card edge connector.

Table 1-1
DC Specifications (BUS I/O - P2)

Signal	IOL (ma)	IOH(ma)	C(pf)
MA0-MA2	-	-	12
MCS0-MCS1	-	-	12
MDACK	Not Connected.	Not Connected.	
MD0-MD7	16	-4	12
IORD*, IOWRT*	-	-	12
MWAIT*	16	-4	12
MDRQT	Not Connected.	Not Connected.	
TDMA	Not Connected.	Not Connected.	
RESET	Not Connected.	Not Connected.	
MCLK	Not Connected.	Not Connected.	
MINTR0, MINTR1	1.6	-0.8	12
OPT0, OPT1	Not Connected.	Not Connected.	
MPST*	Grounded.	Grounded	
+5 VDC (power)	100ma @ 25° C	100ma @ 25° C	

Table 1-2
DC Specifications (Edge Connector - P1)

Signal	IOL (ma)	IOH(ma)	R(OHMS)
TIMECODE IN	-	-	10k
Rate Variance = $\pm 2\%$ of nominal Amplitude 100mV to 5V peak to peak.			
IP CLOCK OUT	1	-1	
AUXA2, AUGA1	<3> -	-	10k
TX(-)	8	-8	
PULSE1	1.6	-0.8	
1PPS	1.6	-0.8	
MOS1, SCK	<2> Do Not Use.	Do Not Use.	

Table 1-3
Signal Definitions (Edge Connector - P1)

Pin Number	Signal/Function
ODD	GROUND
2	Timecode Input
4	Event Input (TTL/CMOS)
6	SCK
8	1PPS Output (CMOS)
10	Pulse Rate 1 Out (CMOS)
12	SYNCH <4>
14	AUXA1 Input (0 to 5 VDC)
16	AUXA2 Input (0 to 5 VDC)
18	10 kHz Timecode Clock <1>
20	MOSI <2>
22	TX(+) Serial Out +
24	TX(-) Serial Out -
26	MISO <2>

- <1> The 10kHz clock is phase locked to the input time code when present, free-running otherwise.
- <2> SCK, MOSI, and MISO support high speed serial I/O used in conjunction with Datum time code generators and video time inserters.
- <3> Auxiliary analog inputs. Each channel is sampled at 8 bit resolution at an effective rate of 1PPS.
- <4> SYNCH is a logic '1' when time code is detected and a logic '0' when flywheeling.

1.3 MECHANICAL DESCRIPTION

The bc330SBX conforms to the specifications of a single-wide expansion module as defined in ANSI/IEEE Standard 959-1988, Figure 18. The SBX connector conforms to Table Seven and Figure 24 of the ANSI document.

A threaded non-conducting spacer is provided with each bc330SBX module for mounting to the baseboard. A 26 pin connector which mates to the card edge connector is also provided with each module. This connector is a solder-less ribbon cable type.

1.4 LEVEL OF COMPLIANCE

The bc330SBX module has an IEEE 959 I/O compliance of D81.

D8 represents an 8 bit module. The 'I' designation indicates that the WAIT* signal line is used. A wait state is only needed when the baseboard is polling the module address corresponding to the 'data ready flag.' A memory contention can occur if the bc330SBX processor is attempting to write to this location while it is being accessed by the baseboard.

No other memory operations require a wait state. The baseboard need not support MWAIT* if the host software is designed to poll the 'data ready flag' twice in succession to circumvent the possible memory contention.

CHAPTER TWO
ADDRESS SPACE

2.0 CONTROL ADDRESS SPACE

The bc330SBX module has a chip select address range as illustrated in Figure 3 of ANSI/IEEE Standard 959-1988. The module address space of the bc330SBX may be modeled as an array of 16 bytes. The lower 8 bytes are selected by MCS0* and the upper 8 bytes are selected by MCS1*.

The bc330SBX software design allocates the lower 8 bytes to data transfer operations, and the upper 8 bytes to control data. In this Section and in Section 2.1, all addresses will be referenced as an offset from the base address, the first address in the 16 byte block. Table 2-1 defines the control functions by address offset.

Table 2-1
Control Functions VS Address Offset

Offset	Default	Functions
08H	00H	Timecode Select 0 = Auto detect. 42H = IRIG B only. 43H = 2137 only (OS 1.1 or >).
09H	00H	Mask Register X0H = Event Capture disabled. X1H = Capture on rising edges. X2H = Capture on falling edges. X3H = Capture on both edges. X=0 Do not assert INTRO. X=1 Assert MINTR0.
0AH	00H <Note>	Status Register (read only) X1H = Decoding IRIG B. X3H = Decoding 2137. X=0 Timecode present. X=1 Flywheeling.
0BH	00H	Pulse Rate Control 00H = Pulse rate disabled. 01H = Pulse enabled.
0CH	07H	Heartbeat Rate msbyte.
0DH	D0H	Heartbeat Rate lsbyte.
0EH	00H	Propagation Delay msbyte.
0FH	00H	Propagation Delay lsbyte.

<Note> Also set to 00H by <initialization> command.

CHAPTER TWO

All of the control data bytes are in read/write RAM and may be accessed at any time. The status byte is the only data byte written to by the bc330SBX. All other bytes are considered read only. Likewise, it makes no sense for the baseboard to write data to the status byte location.

The baseboard may write to the control data at any time. Whether or not the control data is used varies as a function of data type. The heartbeat rate is used by the bc330SBX at the end of every pulse period. All other data bytes are only read during the execution of an initialization command. (See Section 2.1.)

On power on (pon) and when a <reset> command is executed, the control data is initialized to the indicated default values.

It is often useful to generate a periodic pulse/interrupt (heartbeat) which is synchronized to the time source signal. The bc330SBX has the ability to generate heartbeat pulses/interrupts between a 30-2000 Hz rate. The heartbeat rate register determines the rate of the pulses/interrupts (in pulses per second). Following a change to the heartbeat rate registers, the user must ‘initialize’ the bc330SBX.

The bc330SBX achieves synchronization of the heartbeats to the time source by computing the heartbeat pulse/interrupt period by dividing the time code period programmed heartbeat rate. The bc330SBX does the heartbeat period calculations in response to the ‘initialize’ command and at power on. The bc330SBX must be decoding time code or ‘flywheeling’ with a valid time code period to insure accurate heartbeat synchronization.

2.1 DATA TRANSFER ADDRESS SPACE

The data transfer address space consists of a sequence of eight bytes starting at the base address. This address space is accessed by MCS0*. The first seven bytes are dedicated to data and the last byte at offset 07H is reserved as a command byte. This byte is also referred to as a ‘data ready flag byte’ when the baseboard is operating in a polled response mode.

The baseboard requests specific data from the bc330SBX by writing a coded request to offset 07H. The baseboard must then wait for the command byte to be modified by the bc330SBX firmware to indicate that the requested data is available at offset locations 00H through 06H. The data format is defined in this section.

Note: Polling rates of the command register must not exceed 500 kHz.

The following command bytes have been defined for OS 1.0. Additional command bytes may be added in future versions of the bc330SBX firmware.

Com	ready	data		
<u>byte</u>	<u>flag</u>	<u>offset</u>	<u>bits 7-4</u>	<u>bits 3-0</u>

<Requests current time of day. Request time logged as the time when 80H was written to offset 07H.>

80H	00H	0 /	seconds tens	/	seconds units
		1 /	minutes tens	/	minutes units
		2 /	hours tens	/	hours units
		3 /	days tens	/	days units
		4 /	DH1 DH0 0 C20	/	C19 C18 C17 C16
		5 /	C07 C06 C05 C04	/	C03 C02 C01 C00
		6 /	C15 C14 C13 C12	/	C11 C10 C09 C08

C20-C00 = Binary 0.5 microsecond count.

DH1-DH0 = Days of hundreds value (0, 1, 2, 3).

<Request last logged event time. Event time logged on programmed edge, positive or negative or both.>

81H 01H offsets 0-6 same as above

<Clear event capture. Event capture is disabled after each event until the command is executed.>

82H	02H	0 /	time code period mod 65536 lsb
		1 /	time code period mod 65536 msb
		2 /	AUXA1 data byte
		3 /	AUXA2 data byte

MINTR0 is cleared by this command.

The time code period and AUX analog data are returned to facilitate data logging applications which use the event strobe.

<Output auxiliary data.>

83H	03H	0 /	time code period mod 65536 lsb
		1 /	time code period mod 65536 msb
		2 /	AUXA1 data byte
		3 /	AUXA2 data byte
		4 /	AGC level
		5 /	reserved
		6 /	reserved

CHAPTER TWO

<Initialization command>

90H 10H no associated data

<Reset>

91H 10H no associated data

2.2 LATENCY

This section summarizes the latency associated with the data request commands listed above. These times have been determined experimentally using an AT class computer equipped with an SBX bus adapter module. Latency is defined as the time between the initiation of a command (writing to offset 07H) and the detection of the 'ready flag' (offset 07H modified by the bc330SBX firmware).

Command	Typ(msec)	Max(msec)
80H	160	200
81H	110	160
82H	60	100
83H	60	100

CHAPTER THREE

DATA AND CONNECTOR ASSIGNMENTS

3.0 USING TIME CODE PERIOD DATA

The period of the input time code is provided on response to commands 82H and 83H. The return value is the count remaining in a 16 bit counter at the end of a time code second. The counter is reset at the beginning of each detected time code second. If the bc330SBX crystal and the source time code used the same crystal reference, then the return value will be different, reflecting the fact that the two time-bases are not the same. By providing this modulus the bc330SBX allows the user to correct the 0.5 μ sec count data, and remove the small inaccuracies associated with differing crystal frequencies.

Suppose that the period value returned is 35000. This value is 1080 greater than 33920. Furthermore, suppose that the data corresponding to a logged event is returned as follows:

offset	0	36H	(seconds = 36)
offset	1	24H	(minutes = 24)
offset	2	10H	(hours = 10)
offset	3	44H	(days = 144)
offset	4	25H	(0010 0101)
offset	5	67H	(0110 0111)
offset	6	38H	(0011 1000)

$$\begin{aligned} 0.5 \mu\text{sec counts} &= 0 \ 0101 \ 0011 \ 1000 \ 0110 \ 0111 \\ &= 342119 \end{aligned}$$

$$\begin{aligned} \text{uncorrected minor time} &= 342119 / 2E6 \\ &= 0.171059 \text{ seconds} \end{aligned}$$

$$\begin{aligned} \text{corrected minor time} &= 342119 / (2E6+1080) \\ &= 0.170967 \text{ seconds} \end{aligned}$$

$$\text{correction} = 92 \text{ microseconds}$$

$$\begin{aligned} \text{uncorrected event time} &= 144 \ 10:24:36.171059 \\ \text{corrected event time} &= 144 \ 10:24:36.170967 \end{aligned}$$

Accurate event logging and current time reporting are maintained during periods of code loss because the bc330SBX continues to update its internal time-base using the drift correction calculated when a time code was present.

3.1 SERIAL PORT DATA

The serial output data lines TX(+) and TX(-) may be used to drive both the RS-422 and RS-232-C receiver inputs. The RS-422 connections are simply made according to the respective polarity indicated. An RS-232-C receiver, such as a PC serial input, can be driven by connection TS(-) to the RX input pin. The data pacing signals RTS, CTS, DSR, and DTR may need to be jumpered depending on the specific terminal emulation software in use.

The serial port broadcasts in an ASCII format suitable for direct terminal display. This port is very useful for diagnostic purposes. The bc330SBX broadcasts time, measured code period, code detection status, code search status, software version and date code, AGC slice level, and control byte information over this port. The data stream may easily be parsed for a specific data item.

The serial port parameters are as follows:

9600 baud / 8 data bits / 1 stop bit / no parity

3.2 SBX CONNECTOR ASSIGNMENTS (P2)

Table 3-1 summarizes the bc330SBX module SBX bus signal utilization.

**Table 3-1
P2 Connector Assignments**

Pin	Mnemonic	Use	Pin	Mnemonic	Use
1	+12V	N	2	-12V	N
3	GND	Y	4	+5V	Y
5	RESET	N	6	MCLK	N
7	MA2	Y	8	MPST*	GND
9	MA1	Y	10	-----	N
11	MA0	Y	12	MINTR1	GND
13	IOWRT*	Y	14	MINTR0	Y
15	IORD*	Y	16	MWAIT*	Y
17	GND	Y	18	+5V	Y
19	MD7	Y	20	MCS1*	Y
21	MD6	Y	22	MCS0*	Y
23	MD5	Y	24	-----	N
25	MD4	Y	26	TDMA	N
27	MD3	Y	28	OPT1	N
29	MD2	Y	30	OPT0	N
31	MD1	Y	32	MDACK*	N
33	MD0	Y	34	MDRQT	N
35	GND	Y	36	+5V	Y

CHAPTER FOUR

ADJUSTMENT

4.0 ADJUSTMENT

The bc330SBX has only a single adjustment which should never require alteration by the user. This section outlines a method for correctly setting the value of this adjustment, variable resistor R1. The following steps assume that the bc330SBX is correctly mounted on a baseboard and is exposed to allow access by an oscilloscope probe. A source of IRIG B time code is required.

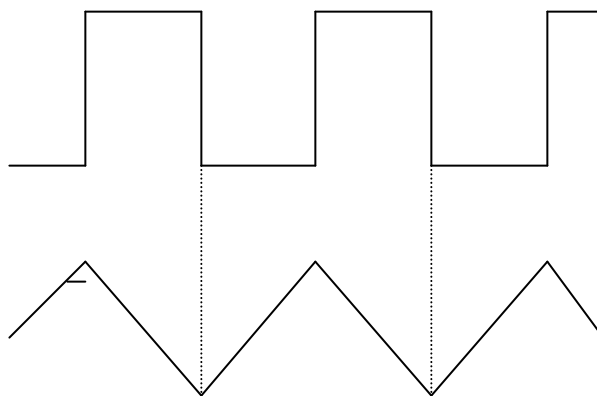
Select an IRIG B time code by writing a 'B' (42H) to offset location 08H. (MCS1* address 0.) This step forces the bc330SBX to search for a 1000 Hz carrier frequency only.

Input the IRIG B time code to pin #2 of edge connector P1.

Use pin #16 of U3 as the input to channel A of a dual channel oscilloscope. Use the reference carrier selected in the above step as the input to channel B of the oscilloscope. Use channel A as the oscilloscope horizontal synch input.

Adjust R1 so that the negative going transitions on pin #16 are centered on the negative "peaks" of the carrier. See figure 4-1 below.

Figure 4-1
Phase Lock Loop Adjustment



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CHAPTER FIVE

DRAWINGS

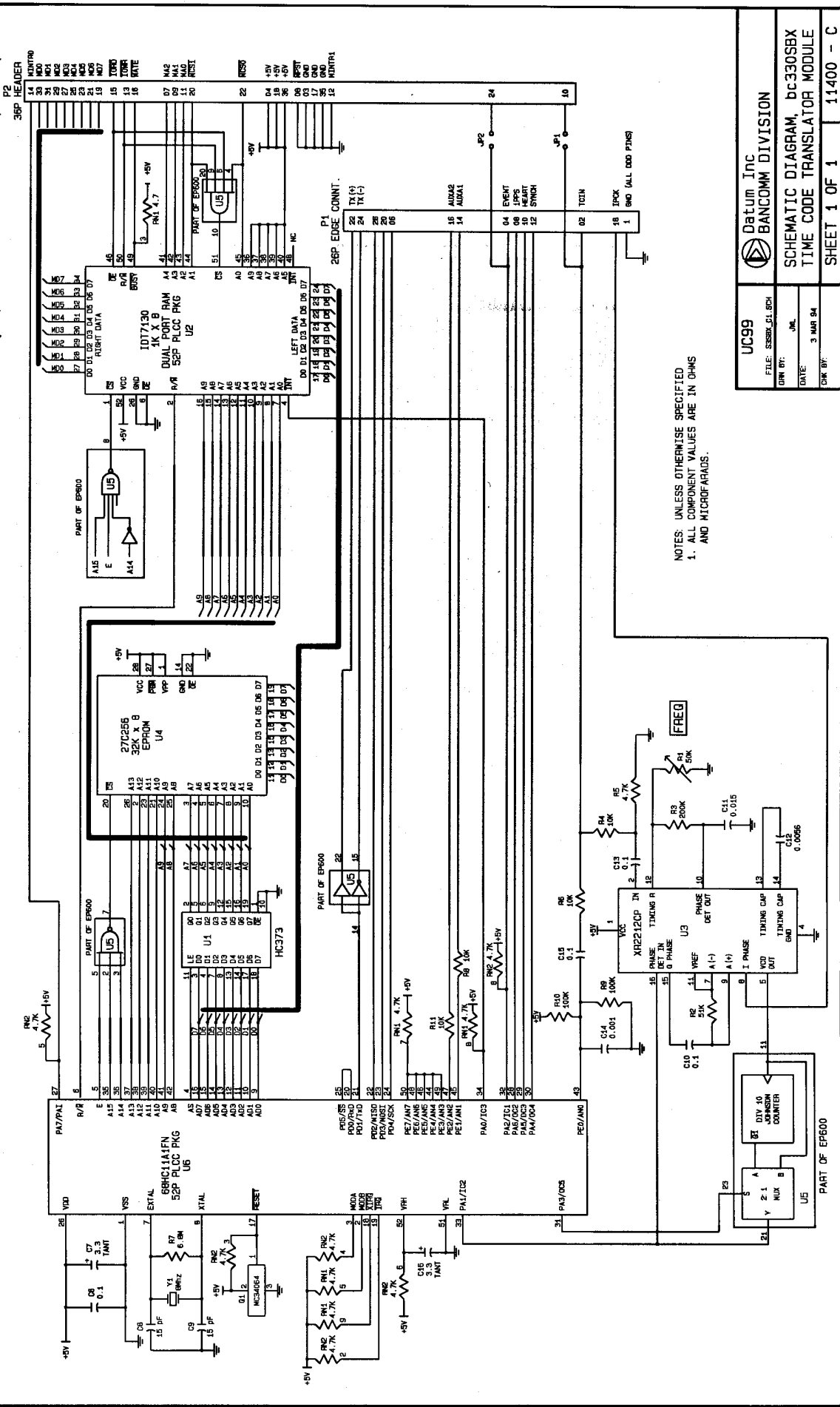
5.0 DRAWINGS

The drawings listed below can be found on the pages following page 6-2.

Title	Number	Revision
Assembly bc330SBX Time Code Translator	11403	C
Schematic Diagram bc330SBX Time Code Translator Module	11400	C

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REV	DESCRIPTION	DATE	APPROVED
A	FIRST RELEASED	6-26-90	DM
B	REV PER ECOF 179	8-31-90	DM
C	REV PER ECOF 237	3-03-94	PH

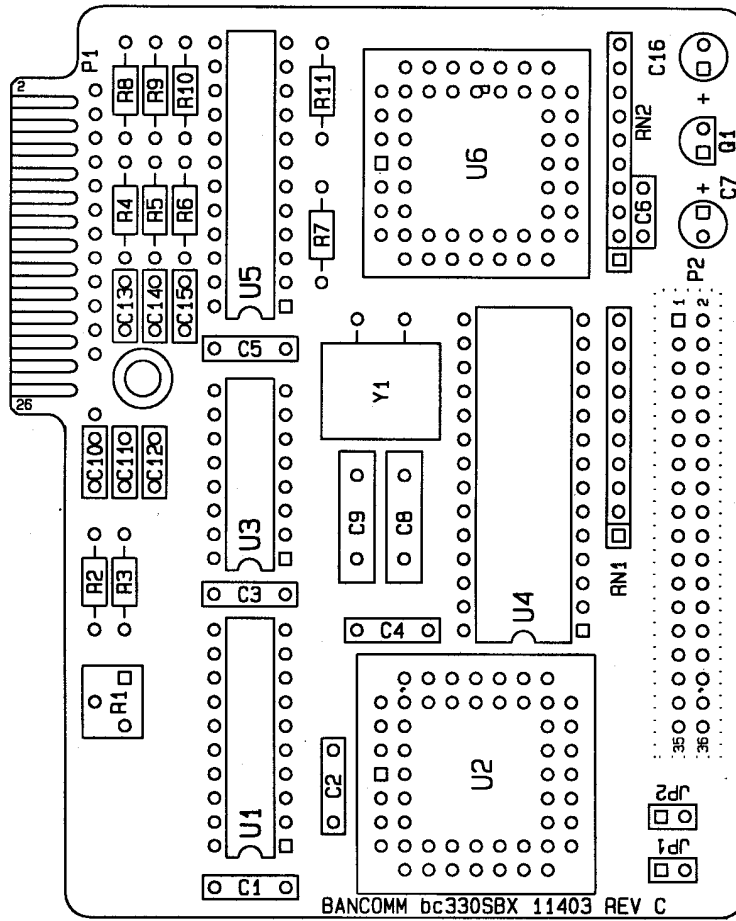


NOTES: UNLESS OTHERWISE SPECIFIED
 1. ALL COMPONENT VALUES ARE IN OHMS AND MICROFARADS.

UC99	Datum Inc	11400 - C
FILE: ESSBX.G1.RCH	BANCOMM DIVISION	
DRW BY: JML	SCHEMATIC DIAGRAM, bc330SBX	
DATE: 3 MAR 84	TIME CODE TRANSLATOR MODULE	
CHK BY:	SHEET 1 OF 1	

REVISIONS

LTR	DESCRIPTION	DATE	APPVD
A	FIRST RELEASED	06/29/90	D.W.
B	REV PER ECO# 179	08/31/90	D.M.
C	REV PER ECO# 237	03/03/94	R.H.



UC099	Datum, Inc. BANCOMM DIVISION
FILE: A3SBX_C1.SCH	ASSEMBLY, bc330SBX
DRWN BY: JWL	TIME CODE TRANSLATOR
DATE: 3 MAR 94	
APP. BY:	SHEET: 1 OF 2 11403 - C

NOTE: P2 CONNECTOR INSTALLED ON SOLDER SIDE.

CHAPTER SIX

PARTS LIST

6.0 PARTS LIST

The parts lists listed below can be found on the pages following page 6-2.

Title	Number	Revision
bc330SBX Time Code Translator	bc11403-1000	D

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Item: BC11403-1000

Description: BC330SBX TIME CODE TRANSLATOR

Revision: D

Oper	WC	Description	Move Hrs	Queue Hrs	Setup Hrs	LbrHrs/Pc	MchHrs/Pc	FixSchHrs	OffsetHrs	Crew Ctl	Size	Pnt	Cell		
10	225	INHOUSE KITTING-OP10	0.00	0.00	0.00	0.000	0.000	?	?	1.00	No				
		Type Item	Revision			Quantity	U/M	Per	Ref	Eff	Date	Obs	Date	BOM	Seq
M		0102-0103 RES: CF, 10K, 1/4W, 5% R4 R6 R8 R11				4.00000	EA	U	I						?
M		0102-0104 RES: CF, 100K, 1/4W, 5% R9 R10				2.00000	EA	U	I						?
M		0102-0204 RES: CF, 200K, 1/4W, 5% R3				1.00000	EA	U	I						?
M		0102-0472 RES: CF, 4.7K, 1/4W, 5% R5				1.00000	EA	U	I						?
M		0102-0513 RES: CF, 51K, 1/4W, 5% R2				1.00000	EA	U	I						?
M		0102-0685 RES: CF, 6.8M OHM, 1/4W, 5% R7				1.00000	EA	U	I						?
M		0128-0472 RES: NET, 4.7K, 9R, SIP10 RN1 RN2				2.00000	EA	U	I						?
M		0154-0503-1 RES: POT, 50K, 1T, 1/2W R1				1.00000	EA	U	I						?
M		0220-0335-1 CAP: TANT ELECT, 3.3UF, 35V, 10% C7 C16				2.00000	EA	U	I						?

Item: BC11403-1000

Description: BC330SBX TIME CODE TRANSLATOR

Revision: D

Oper	WC	Description	Move Hrs	Queue Hrs	Setup Hrs	LbrHrs/Pc	MchHrs/Pc	FixSchHrs	OffsetHrs	Crew Ctl	Size	Pnt	Cell
Type	Item	Revision	Quantity	U/M	Per	Ref	Eff	Date	Obs	Date	BOM	Seq	
M	0226-0102-2		1.00000	EA	U	I							?
	CAP: 1000PF, 100V, 10%, X7R, .20LS												
	C14												
M	0226-0104-4		4.00000	EA	U	I							?
	CAP: 0.1UF, 50V, 20%, X7R, .20LS												
	C6 C10 C13 C15												
M	0226-0104-5		5.00000	EA	U	I							?
	CAP: 0.1UF, 50V, 20%, Z5U, .30LS												
	C1 C2 C3 C4 C5												
M	0226-0153		1.00000	EA	U	I							?
	CAP: 0.015UF, 100V, 10%, X7R, .20LS												
	C11												
M	0226-0562		1.00000	EA	U	I							?
	CAP: 5600PF, 100V, 10%, X7R, .20LS												
	C12												
M	0227-0150		2.00000	EA	U	I							?
	CAP: MICA, 15PF, 500V, 5%, .23LS												
	C8 C9												
M	0301-0610-1		1.00000	EA	U	I							?
	IC: EP610-35 DIP24 .3C												
	US (SKT) SEE NOTES												
M	0301-2212		1.00000	EA	U	I							?
	IC: XR2212C DIP16												
	U3												
M	0301-27C2-56		1.00000	EA	U	I							?
	IC: 27C256-150 DIP28												
	U4 (SKT) SEE NOTES												

Item: BC11403-1000

Description: BC330SBX TIME CODE TRANSLATOR

Revision: D

Oper	WC	Description	Move Hrs	Queue Hrs	Setup Hrs	LbrHrs/Pc	MchHrs/Pc	FixSchHrs	OffsetHrs	Crew Ctl				
										Size Pnt Cell				
Type	Item	Revision			Quantity	U/M	Per	Ref	Eff	Date	Obs	Date	BOM	Seq
M	0301-3406-4					1.00000	EA	U	I					?
	IC: MC34064-5 TO-92													
	Q1													
M	0301-HC37-3					1.00000	EA	U	I					?
	IC: 74HC373 DIP20													
	U1													
M	0303-6811-A1					1.00000	EA	U	I					?
	IC: MC68HC11A1 PLCC52 (OBSOLETE)													
	U6 (SKT)													
M	0303-7130					1.00000	EA	U	I					?
	IC: IDT7130LA70 PLCC52													
	U2 (SKT)													
M	1302-0008					1.00000	EA	U	I					?
	CRYSTAL: 8 MHZ SERIES HC-49/U													
	Y1													
M	1701099					1.00000	EA	U	I					?
	P. C. BOARD 11402C													
	PCB1													
M	1702-0036					1.00000	EA	U	I					?
	CONN: 36P 2X18 PLUG ST													
	P2 SEE NOTES													
M	1708-0052					2.00000	EA	U	I					?
	SOCKET: IC 52P PLCC													
	REF U2 U6													
M	1708-3100-28					1.00000	EA	U	I					?
	SOCKET: IC 28P DIP													
	REF U4													

Item: BC11403-1000

Description: BC330SBX TIME CODE TRANSLATOR

Revision: D

Oper	WC	Description	Move Hrs	Queue Hrs	Setup Hrs	LbrHrs/Pc	MchHrs/Pc	FixSchHrs	OffsetHrs	Crew Ctl
										Size Pnt Cell
M		1708-3518 SOCKET: IC 24P DIP .3C				1.00000	EA U I			?
		REF U5								
M		1709-0026 CONN: 26P 2X13 EDGE .100C IDC				1.00000	EA U I			?
		P1 SEE NOTES								
20	327	OPER.-ELEC/MECH ASSY	0.00	0.00	0.00	1.000		0.000	?	? 1.00 No
30	452	PROD. TEST INSP	0.00	0.00	0.00	0.000		0.000	?	? 1.00 No
40	400	TEST	0.00	0.00	0.00	0.500		0.000	?	? 1.00 No

NOTES:
SEE ASSY. DWG# 11403C FOR COMPONENT
LOCATION.

HAREWARE INSTRUCTIONS:
1. LOCATE HOLE IN PCB BETWEEN C12 & C14.
INSTALL A #6-1/4X1/2" NYLON HEX STANOFF
TO BACK SIDE OF PCB USING A #6X3/16
NYLON SCREW.
2. 1709-0026: NOT INSTALLED UNTILL AFTER
TESTING.

MEMORY IC's: THE FOLLOWING MEMORY CHIPS
MUST BE PROGRAMED BEFORE INSTALLATION ON
PC BOARD:
1. 0301-0610-1 EP610 TO U5
PROGRAMMED PER BURN FILE 9520023.
2. 0301-27C2-56 27C256 TO U4
PROGRAMMED PER BURN FILE DT10025.

SPECIAL COMPONENT INSTALLATION:
1702-0036 INSTALL TO BACK SIDE OF PCB.